

# Z05 SYSTEM BLOCK DIAGRAM



CPU CORE / VDDNB  
(ISL6265A)  
PAGE 26

NB\_CORE +1.1V  
(RT8202)  
PAGE 28

+1.1V\_NB  
(RT8202)  
PAGE 27

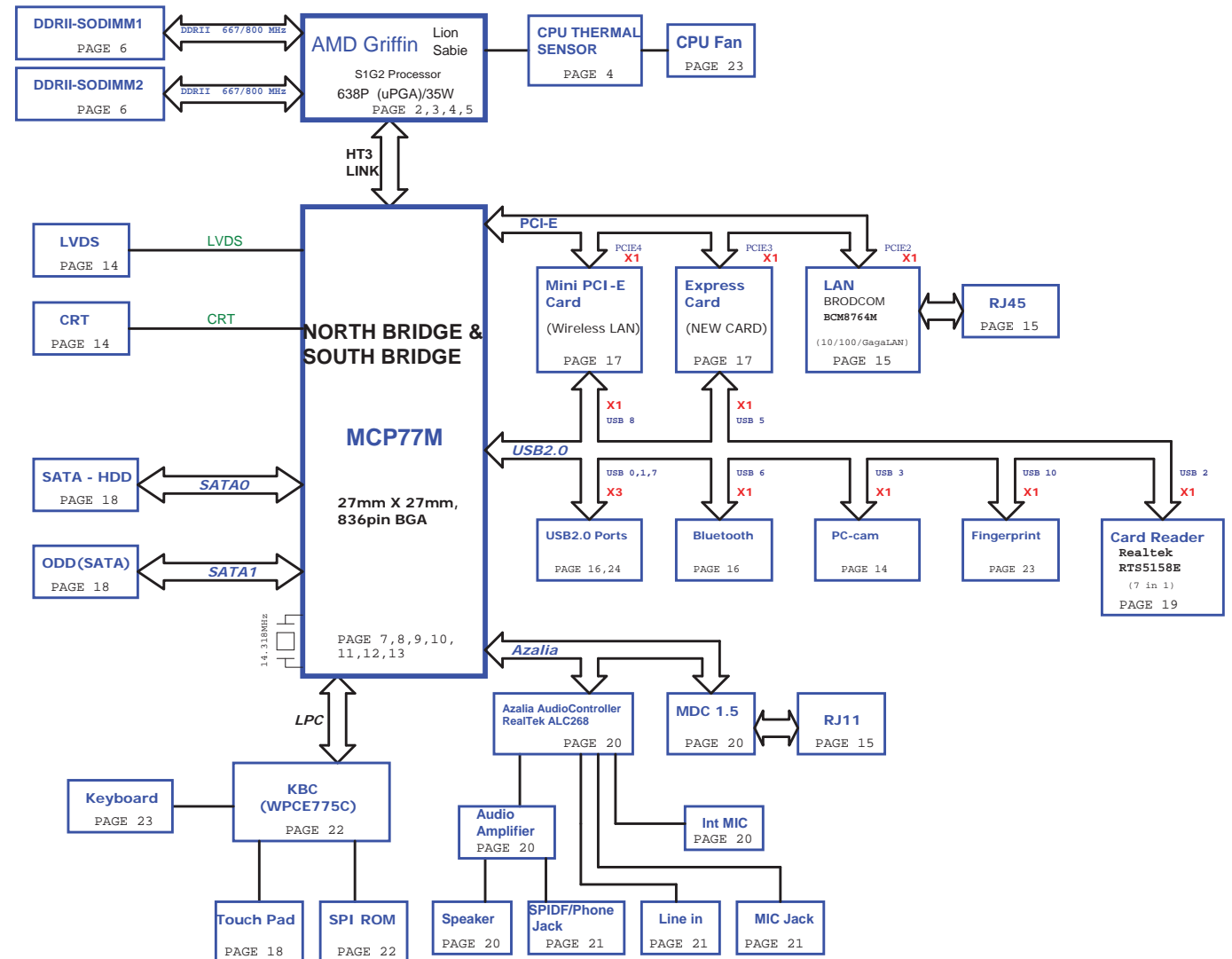
DDR II SMD DR\_VTERM  
1.8VSUS(TPSS1116REGR)  
PAGE 29

SYSTEM POWER  
(ISL6237)  
PAGE 25

SYSTEM CHARGER  
(ISL6251A)  
PAGE 24

## PCB STACK UP

LAYER 1 : TOP  
LAYER 2 : GND  
LAYER 3 : IN1  
LAYER 4 : IN2  
LAYER 5 : VCC  
LAYER 6 : BOT

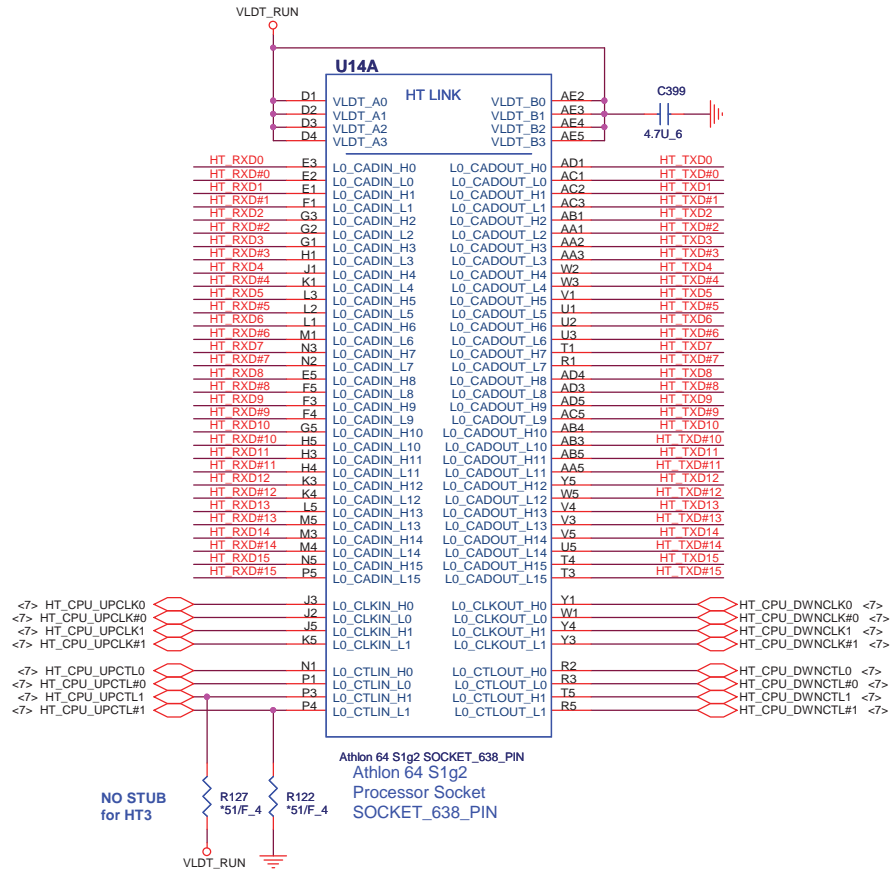


<7> HT\_RXD#[15..0] HT\_RXD[15..0]  
 <7> HT\_TXD#[15..0] HT\_TXD[15..0]

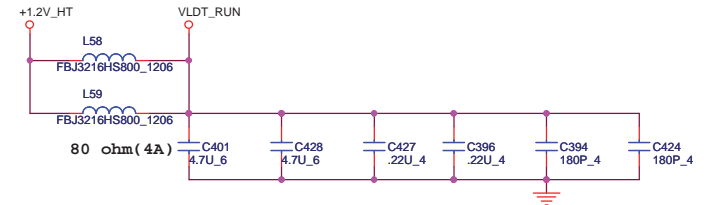


### PROCESSOR HYPERTRANSPORT INTERFACE

VLDT\_Ax AND VLDT\_Bx ARE CONNECTED TO THE LDT\_RUN POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE



Note: on MCP77, (HT=+1.1V) and CPU(HT=+1.2V) and therefore cannot be connected to the same HT power rail.



### LAYOUT: Place bypass cap on topside of board

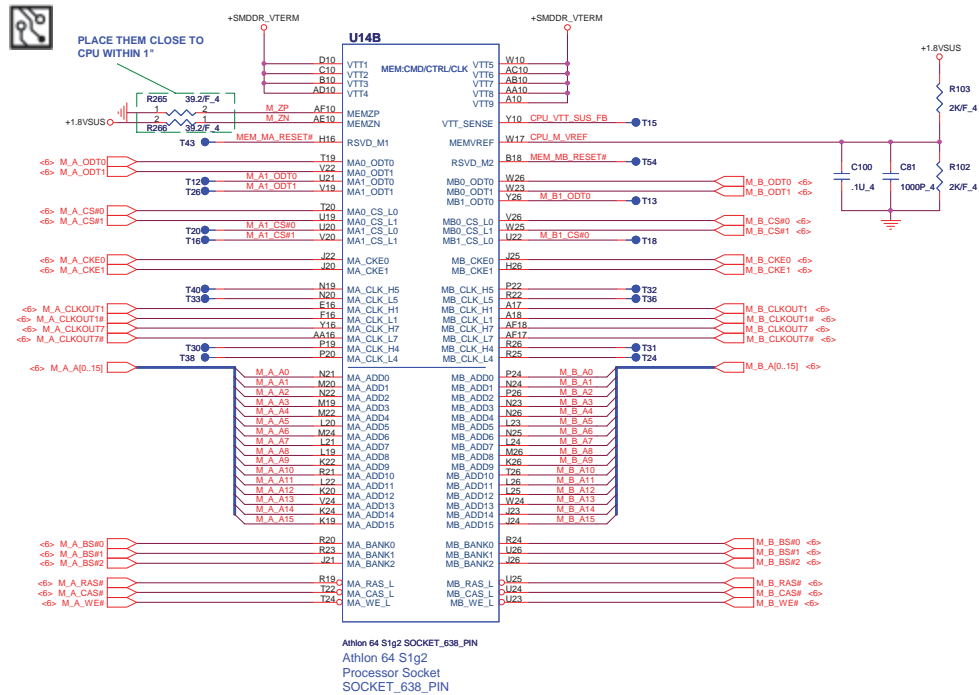
NEAR HT POWER PINS THAT ARE NOT CONNECTED DIRECTLY TO DOWNSTREAM HT DEVICE, BUT CONNECTED INTERNALLY TO OTHER HT POWER PINS  
 PLACE CLOSE TO VLDT0 POWER PINS

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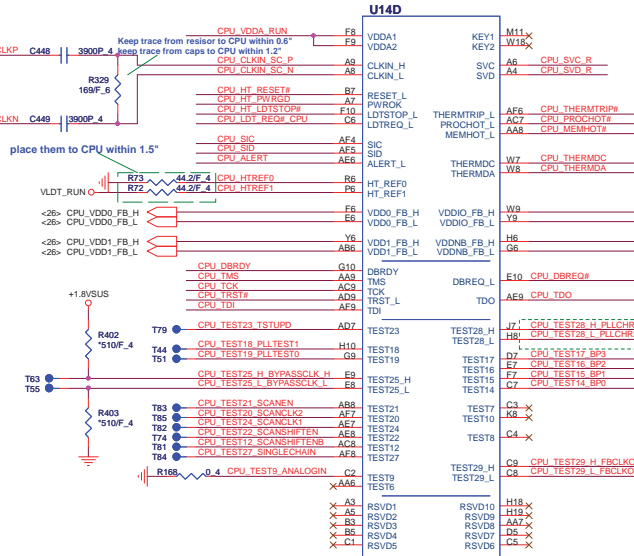
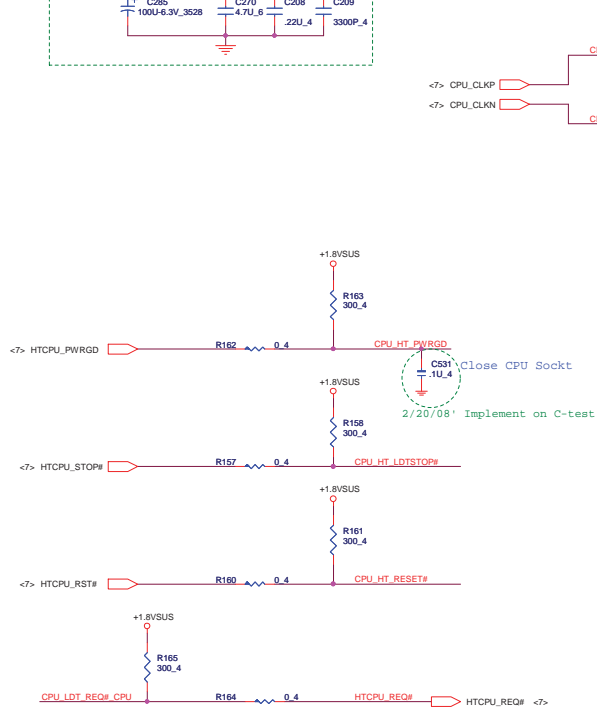
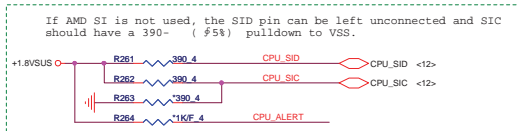
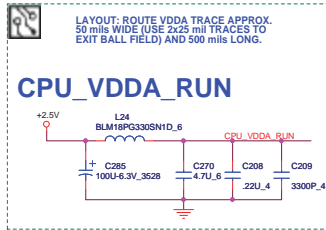
**PROJECT : Z05**

Size	Document Number	Rev
	<b>AMD Griffin HT I/F</b>	1A
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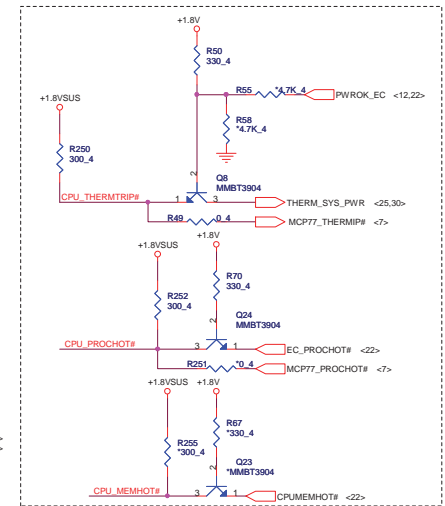
VDD\_VTT\_SUS\_CPU IS CONNECTED TO THE VDD\_VTT\_SUS POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE



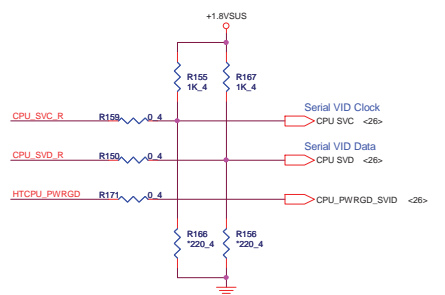
# ATHLON Control and Debug



route as differential as short as possible testpoint under package

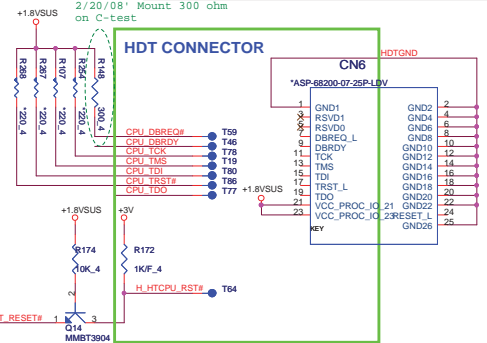
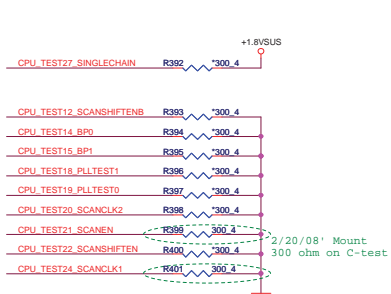
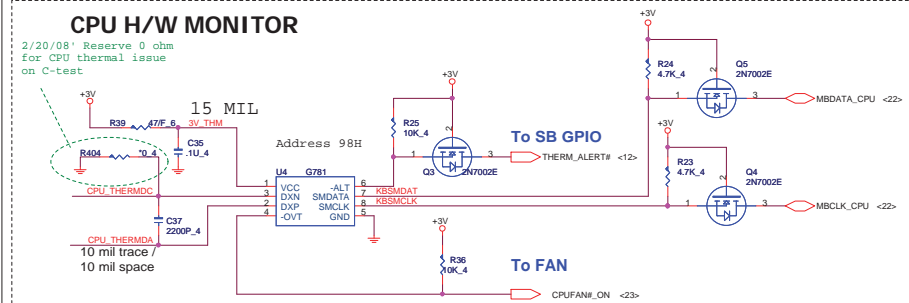


## VID Override Circuit

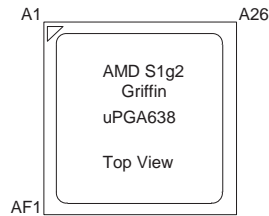
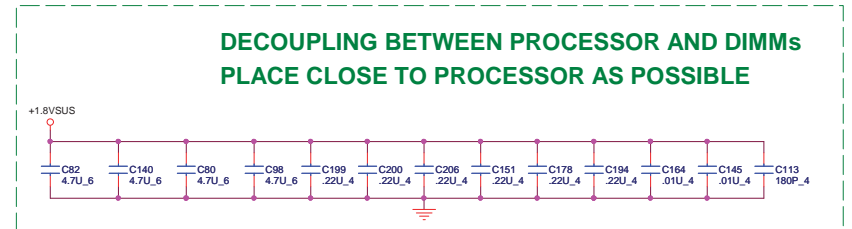
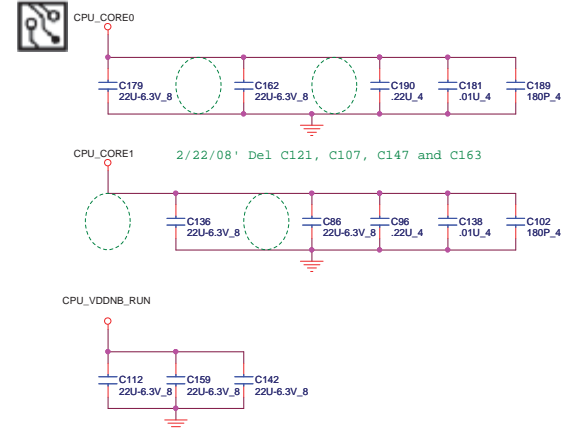
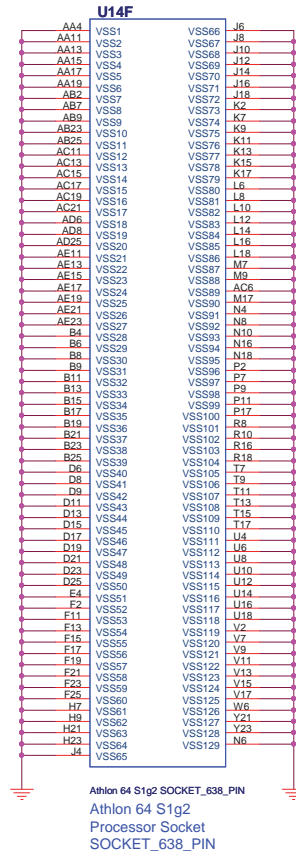
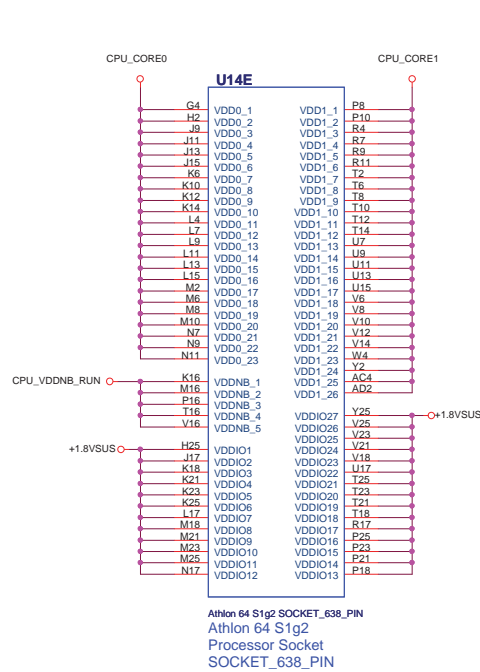


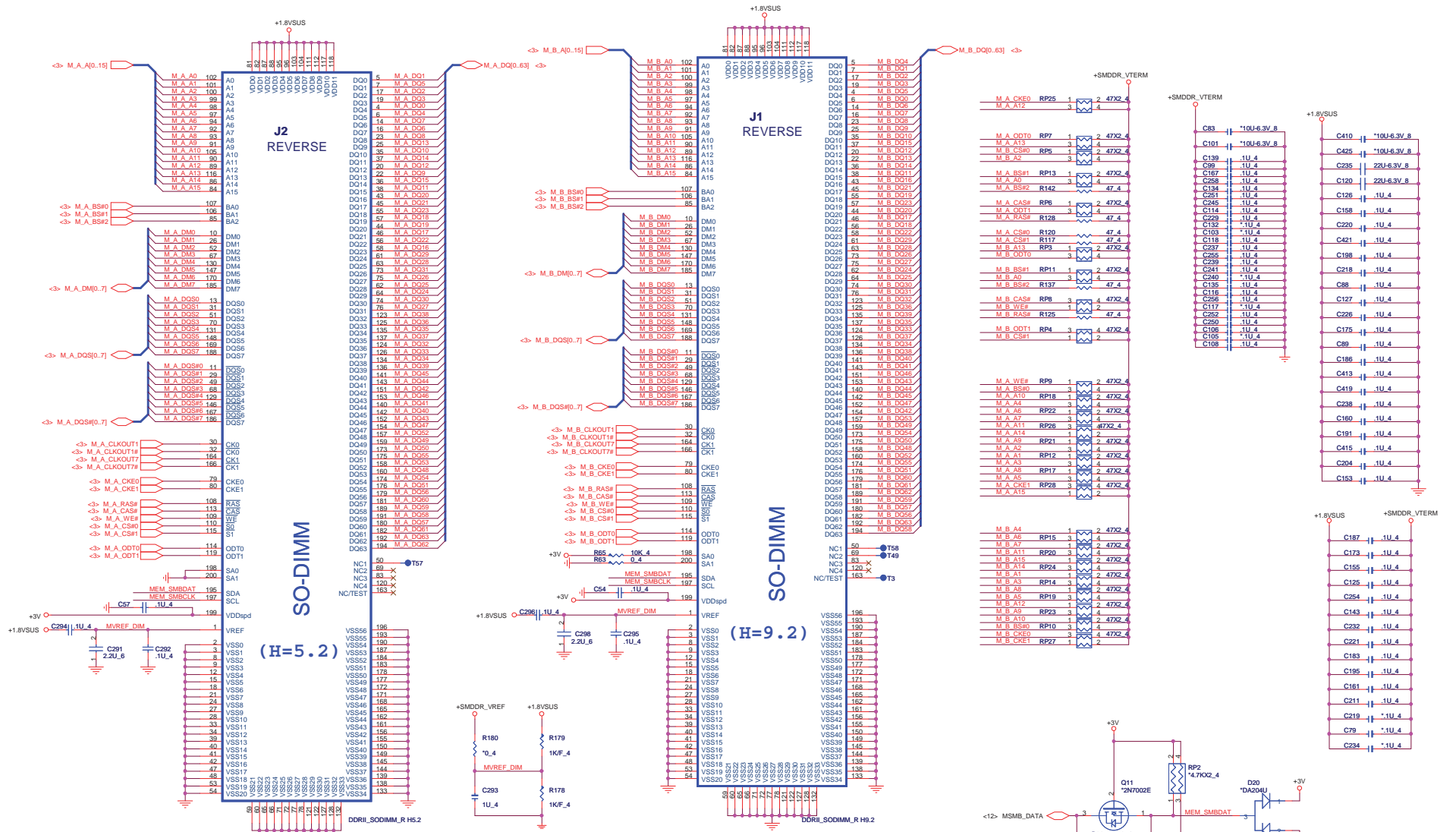
## VFIX MODE

SVC	SVD	Voltage Output(CPU Power)
0	0	1.4V
0	1	1.2V
1	0	1.0V
1	1	0.8V



# PROCESSOR POWER AND GROUND





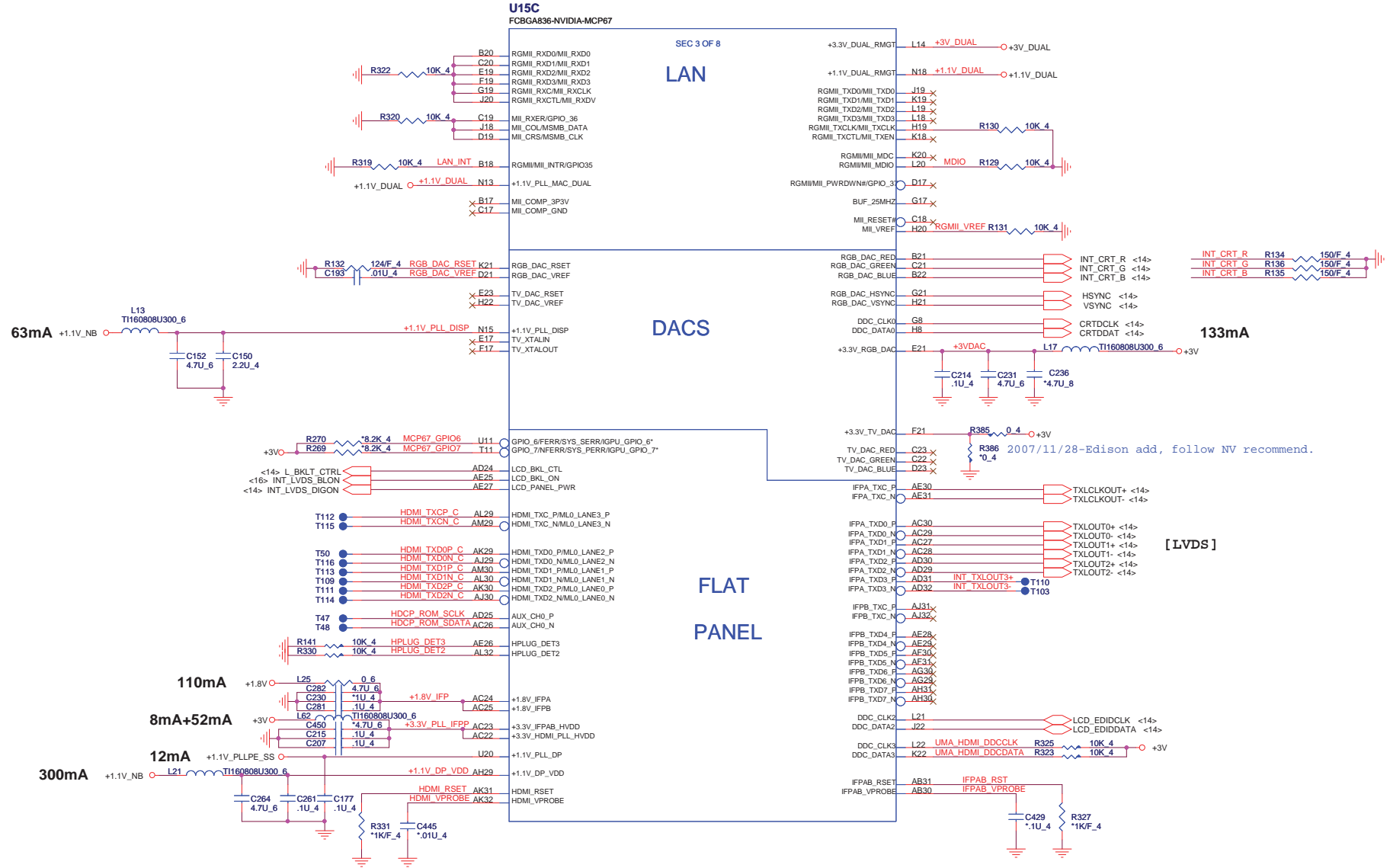












U15E  
FCBG836-NVIDIA-MCP67

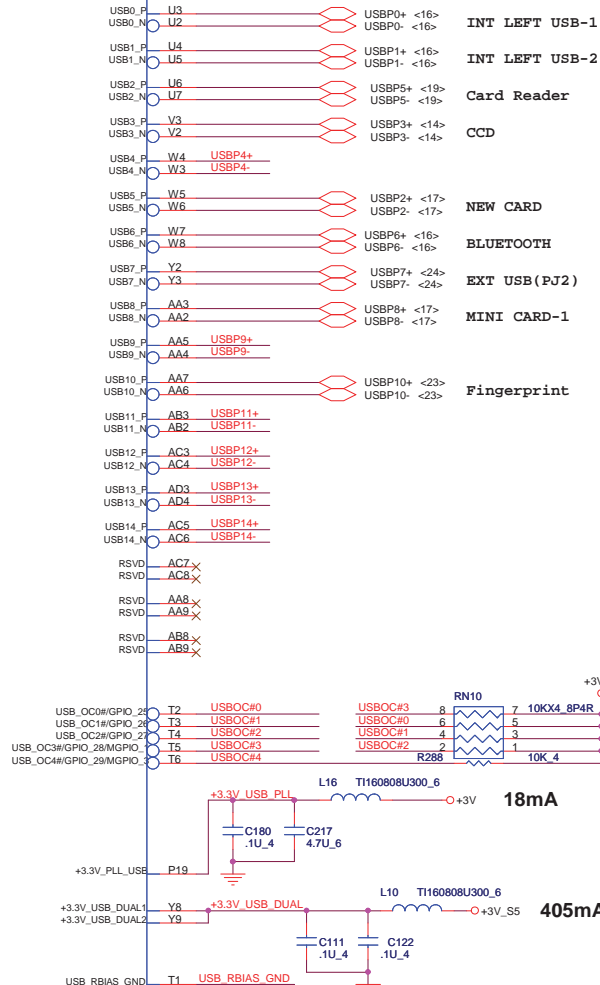
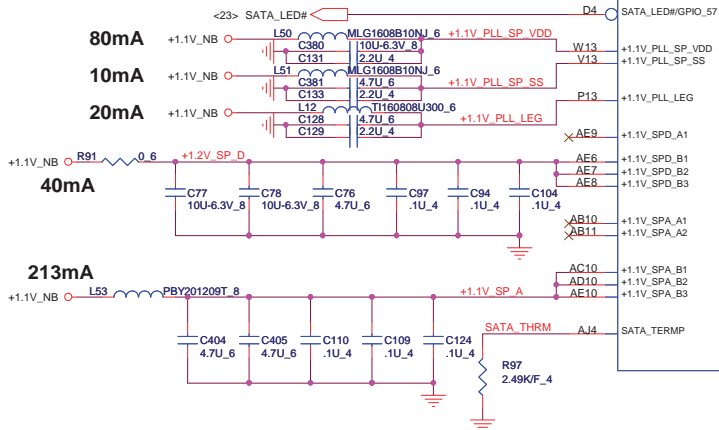
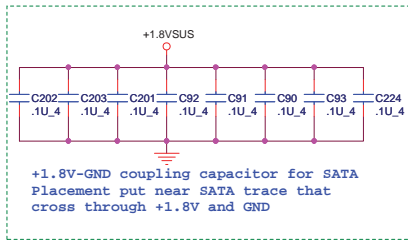
SEC 5 OF 8

SATA

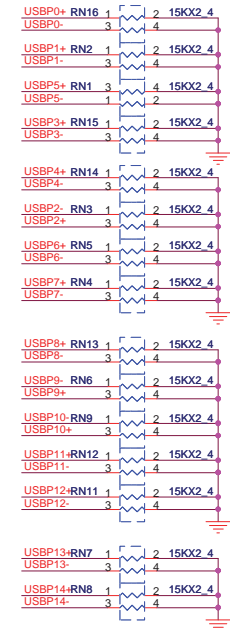
USB

[SATA HDD]

[SATA ODD]



USB PULL-DOWN



2007/11/29: Page11 the  
resistor R87 from 909ohm  
change to 845ohm(follow  
NV suggest)

# U15F FCBGA836-NV/DIA-MCP67

## HDA

## MISC

## HDA

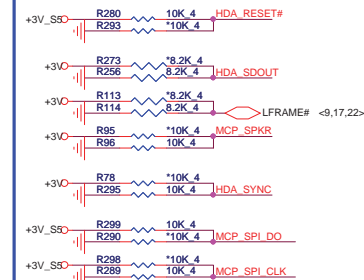
HDA_SDOUT	R74	22 4	HDA_SDOUT_ADO	<20>
HDA_SYNC	R77	22 4	HDA_SDOUT_MDC	<20>
HDA_BITCLK	R285	22 4	HDA_SYNC_ADO	<20>
HDA_RESET#	R292	22 4	HDA_SYNC_MDC	<20>
	R81	22 4	HDA_BITCLK_ADO	<20>
	R86	22 4	HDA_BITCLK_MDC	<20>
	R284	22 4	HDA_RESET#_ADO	<20>
	R291	22 4	HDA_RESET#_MDC	<20>

## EMI Solution

HDA_SDOUT	C373	10P 4
HDA_SYNC	C395	10P 4
HDA_RESET#	C393	10P 4
HDA_BITCLK	C392	10P 4

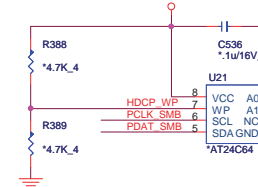
## MCP77 STRAPPING

HDA_RESET# (LAN)	0	MI
HDA_RESET# (LAN)	1	RGMI (DEFAULT)
HDA_SDOUT_R (LFRAM# (BIOS)	0	LPC (DEFAULT)
HDA_SDOUT_R (LFRAM# (BIOS)	01	PCI BIOS
HDA_SDOUT_R (LFRAM# (BIOS)	10	SPI BIOS
HDA_SDOUT_R (LFRAM# (BIOS)	11	RESERVED (SPI)
MCP_SPKR (Boot MODE)	0	USER TABLE (DEFAULT)
MCP_SPKR (Boot MODE)	1	SAFE TABLE
HDA_SYNC_R (SIG CLOCK)	0	14.318MHz (DEFAULT)
HDA_SYNC_R (SIG CLOCK)	1	24MHz
SPI_DO SPI_CLK (SPI CLOCK)	0	31MHz
SPI_DO SPI_CLK (SPI CLOCK)	01	42MHz
SPI_DO SPI_CLK (SPI CLOCK)	10	25MHz
SPI_DO SPI_CLK (SPI CLOCK)	11	1MHz

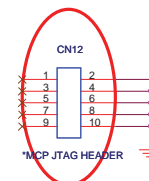


## Acer Suggest Reserve HDCP EEPROM 2007/12/05

## HDCP EEPROM



## NO PN



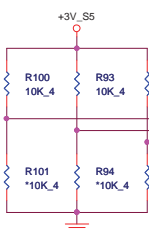
## M/B ID for 14"/17"

ID0	ID1	ID2	M/B
0	0	0	17" D
0	0	1	X
0	1	0	15" D
1	0	0	15" U
1	0	1	14" Dual Core CPU & MXM
1	1	0	14" Dual Core CPU & UMA
1	1	1	14" Single Core CPU & UMA

## SMB/I2C PULL-UP

PCLK_SMB	R89	2.7K 4
PDAT_SMB	R88	2.7K 4
SMB_ALERT#	R294	2.7K 4

MSMB_CLK	R82	2.7K 4
MSMB_DATA	R271	2.7K 4




Delay 10ms  
after S5 powerOK

2007/11/28-Edison: Removethese part  
R315, R317, R326, R324, C423, Q28, Q29

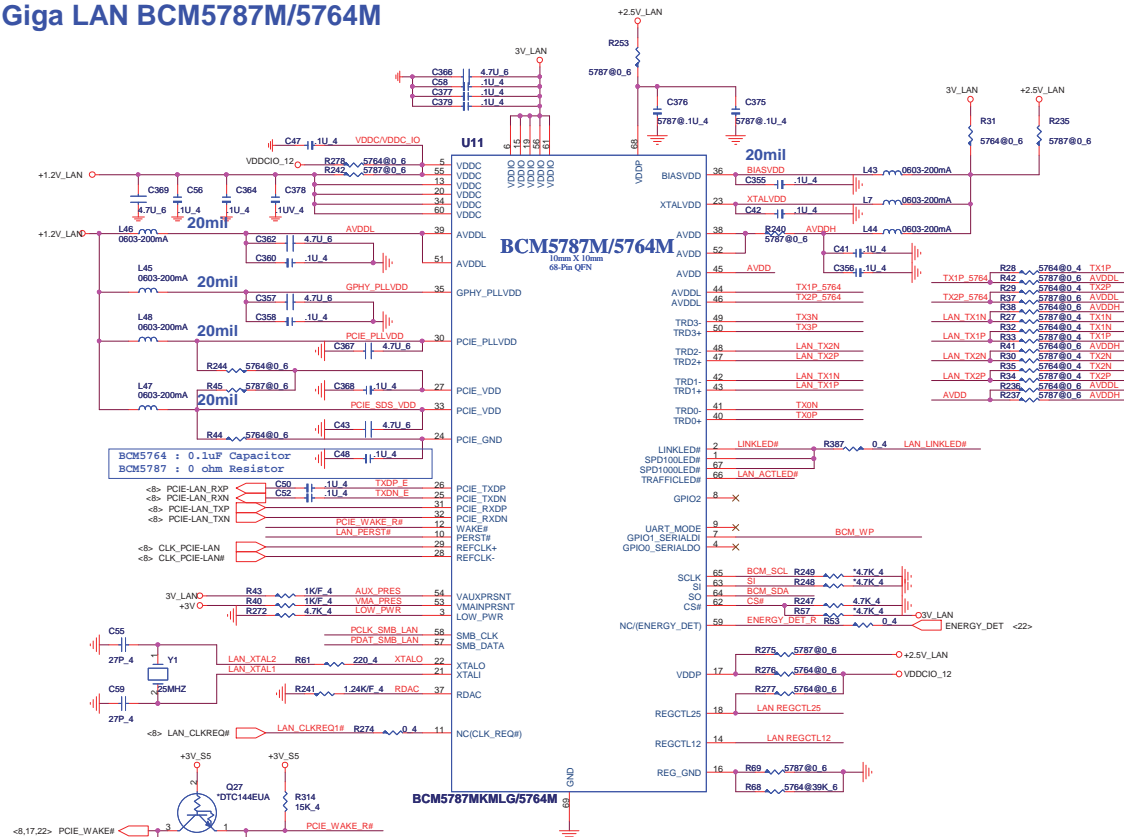


SINGLE\_CH

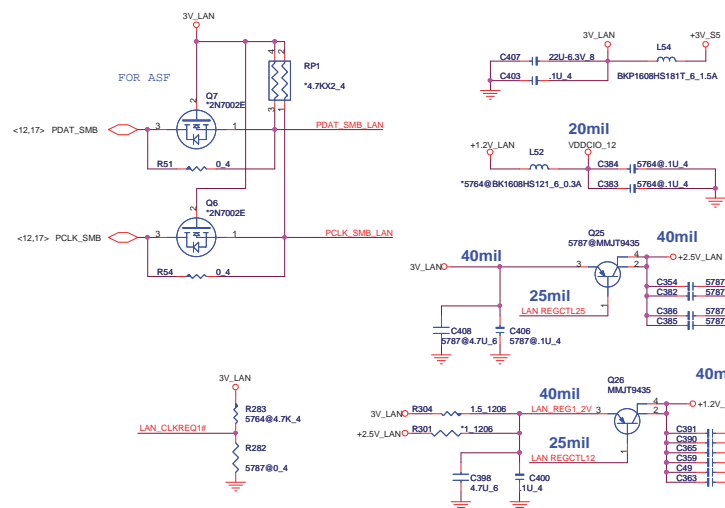


 <b>Quanta Computer Inc.</b> <b>PROJECT : Z05</b>		
Size	Document Number	Rev
	<b>LVDS/CRT/PC-Camera</b>	<b>1A</b>
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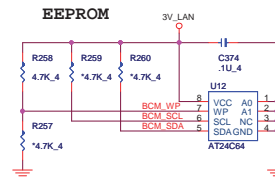
**Giga LAN BCM5787M/5764M**



## LAN POWER

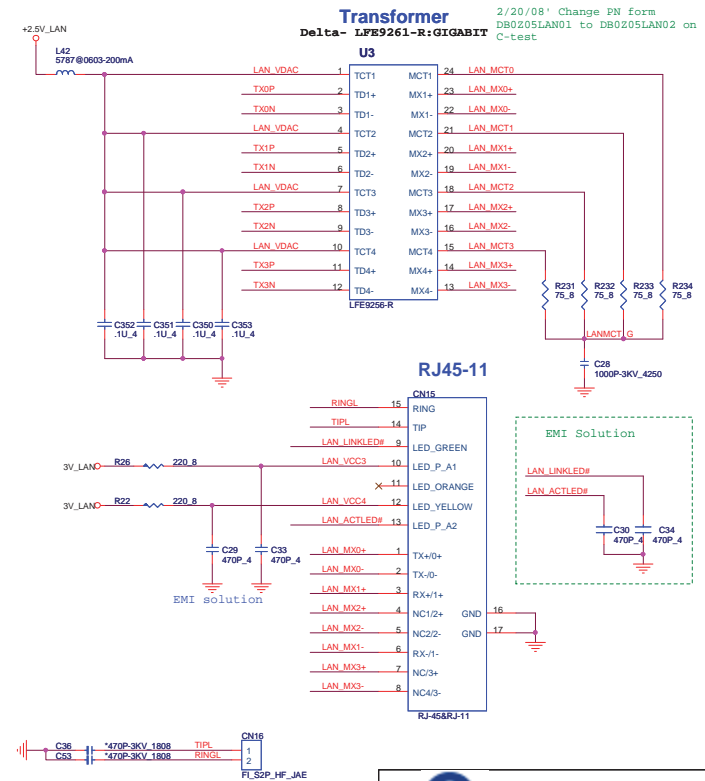


## EEPROM



## EEPROM Strapping

	SO	SI	CS#	SCL#
24c64	1	1	0	1



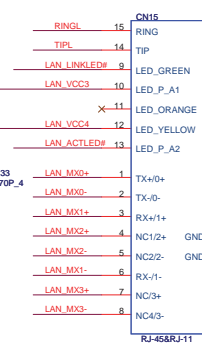
### Delete LAN within DOCK Selector

## Transformer

Delta- LFE9261-R:GIGABIT

2/20/08' Change PN form  
DB0Z05LAN01 to DB0Z05LAN02 on  
C-test

## RJ45-11



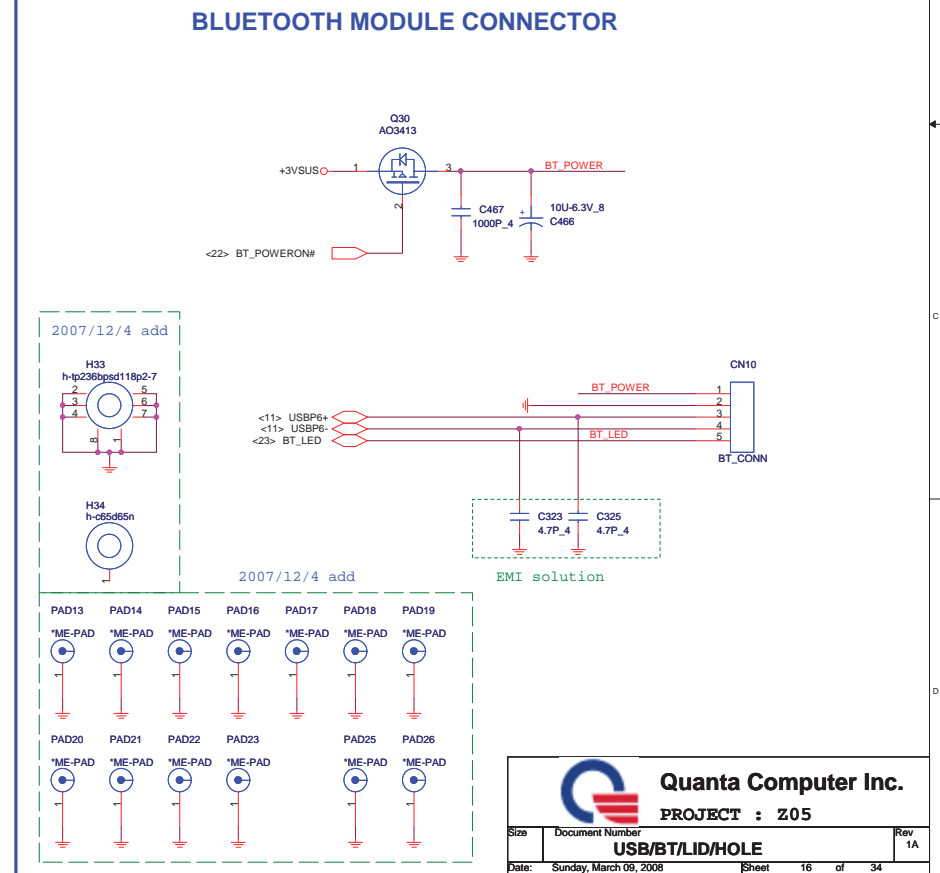
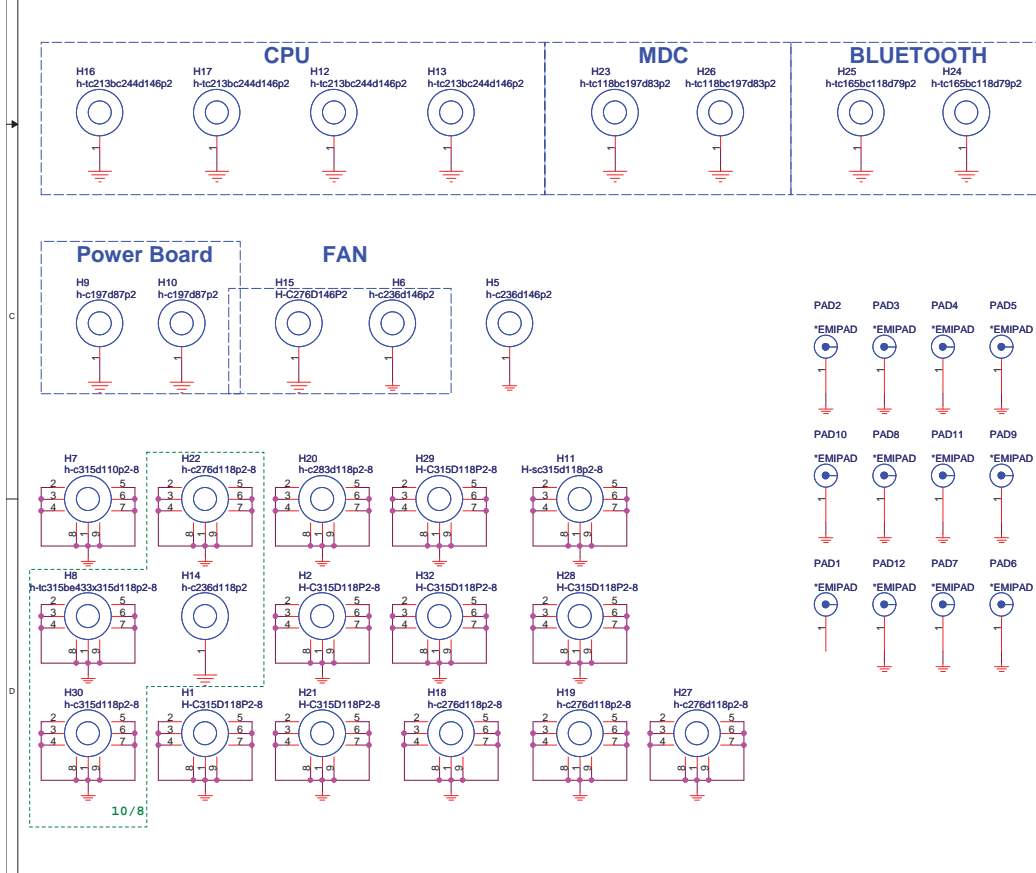
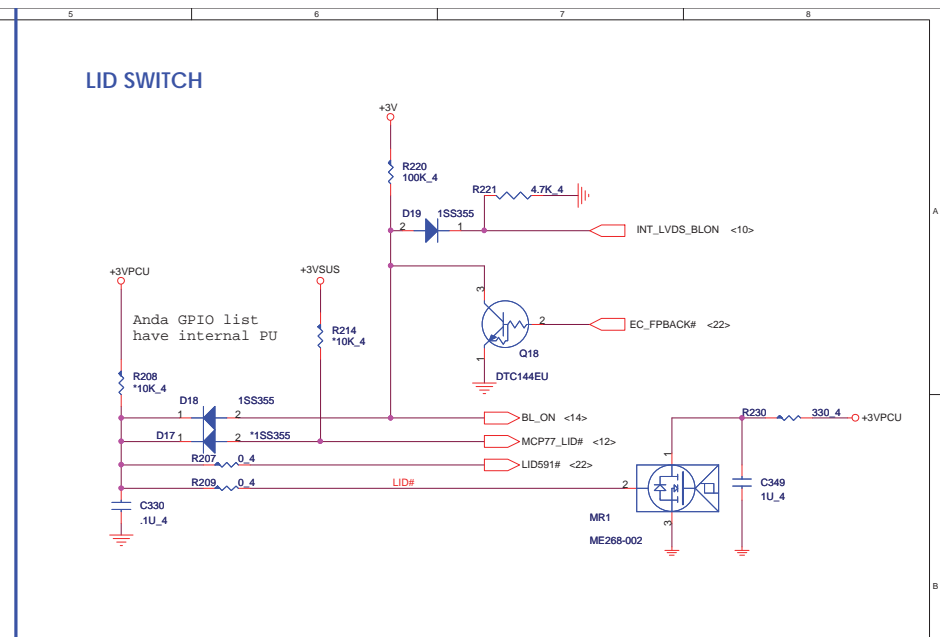
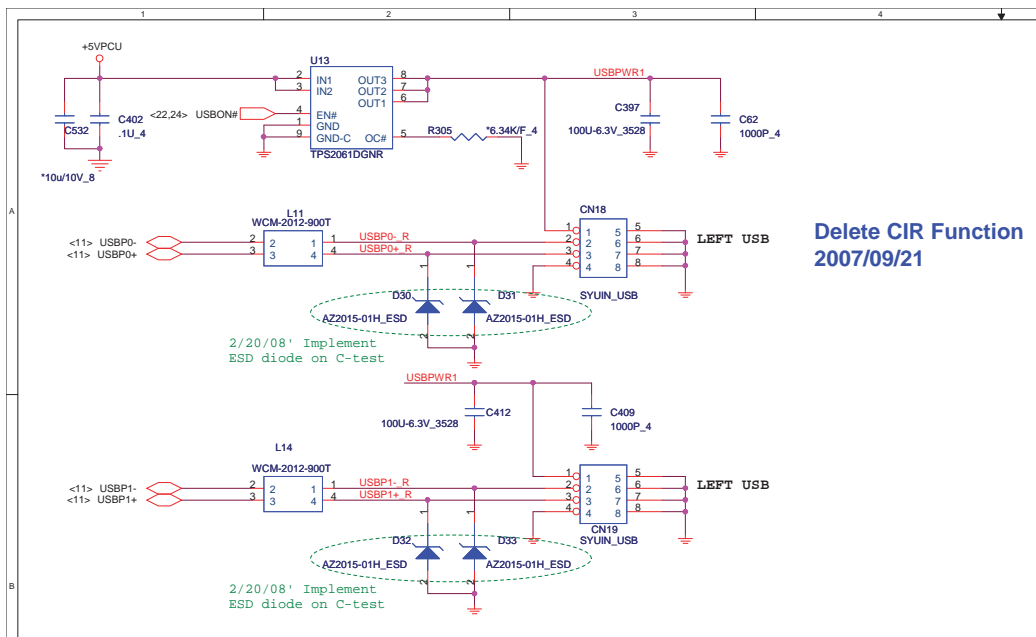
The diagram shows two signals, LAN\_LINKED# and LAN\_ACTED#, connected to a common node. This node is connected to two capacitors, C30 and C34, which are connected to ground. The capacitors are labeled 470P\_4.



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**PROJECT : Z05**

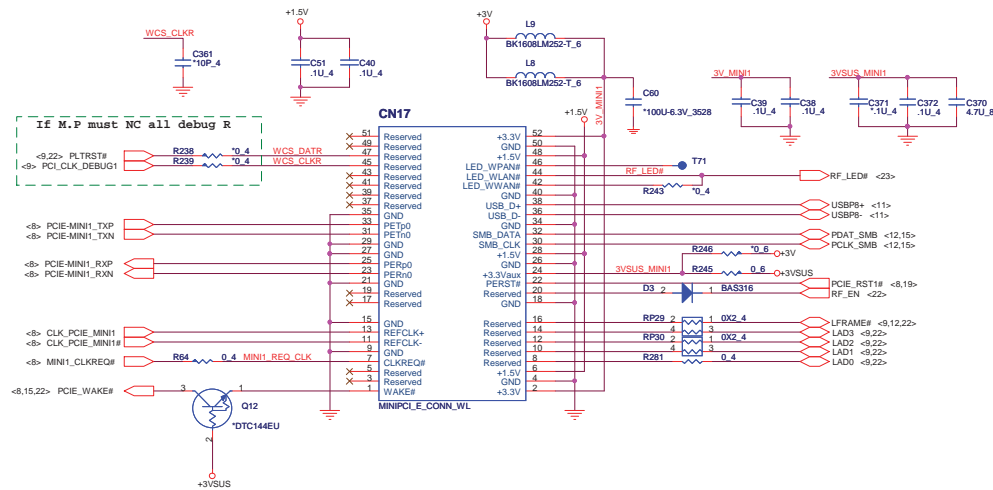
Size	Document Number	Rev
	<b>GigaLAN BCM5787/RJ45 &amp; RJ11</b>	1A
Date:	Friday, March 07, 2008	Sheet 15 of 34





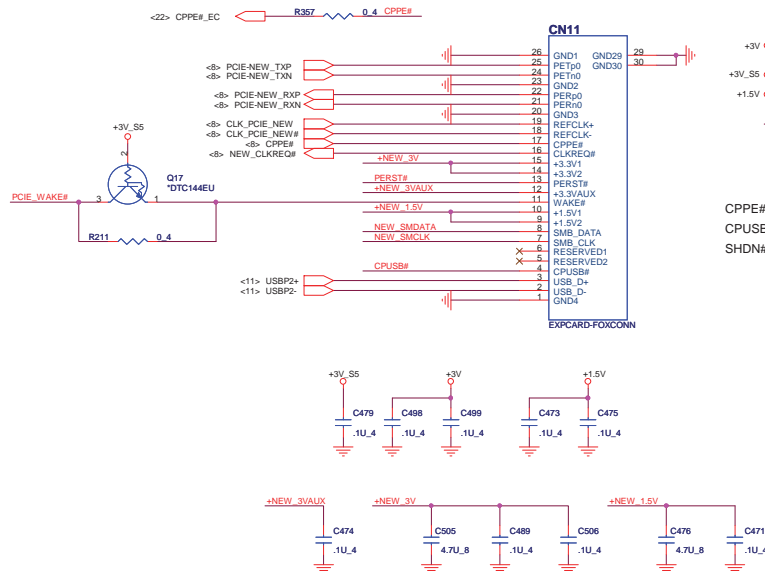
## MINI-Card

### MINI-Card Port-1

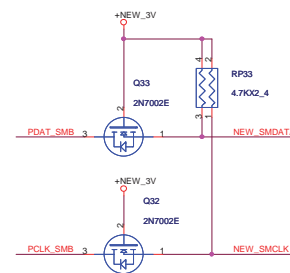
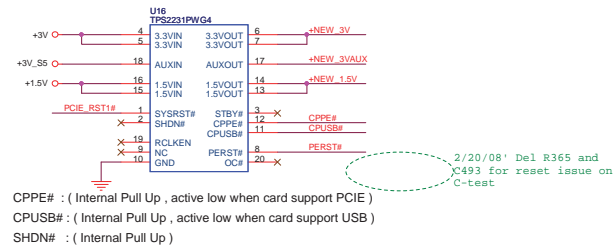


### Delete MINI-Card Port-2

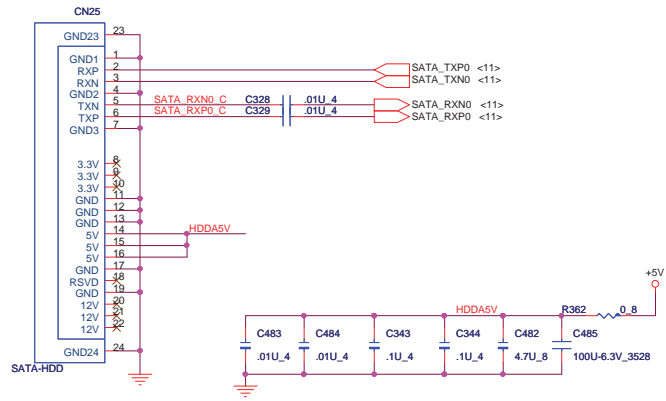
### New card



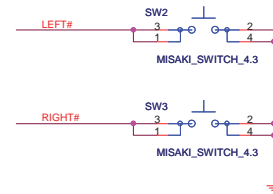
## NEW CARD'S POWER SWITCH



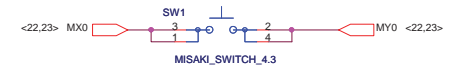
## SATA HDD



## TP SWITCH

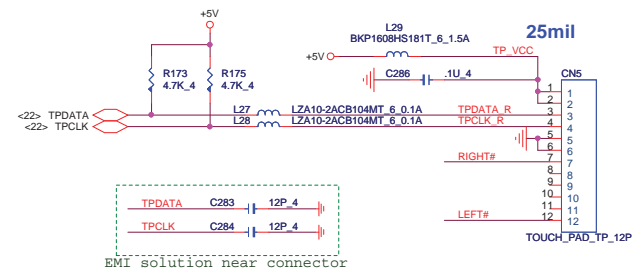


## E-KEY

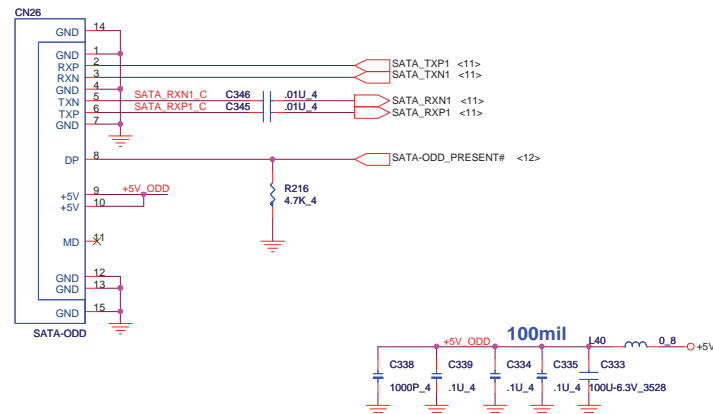


MX0 MY0:E-Key

## TP CONN



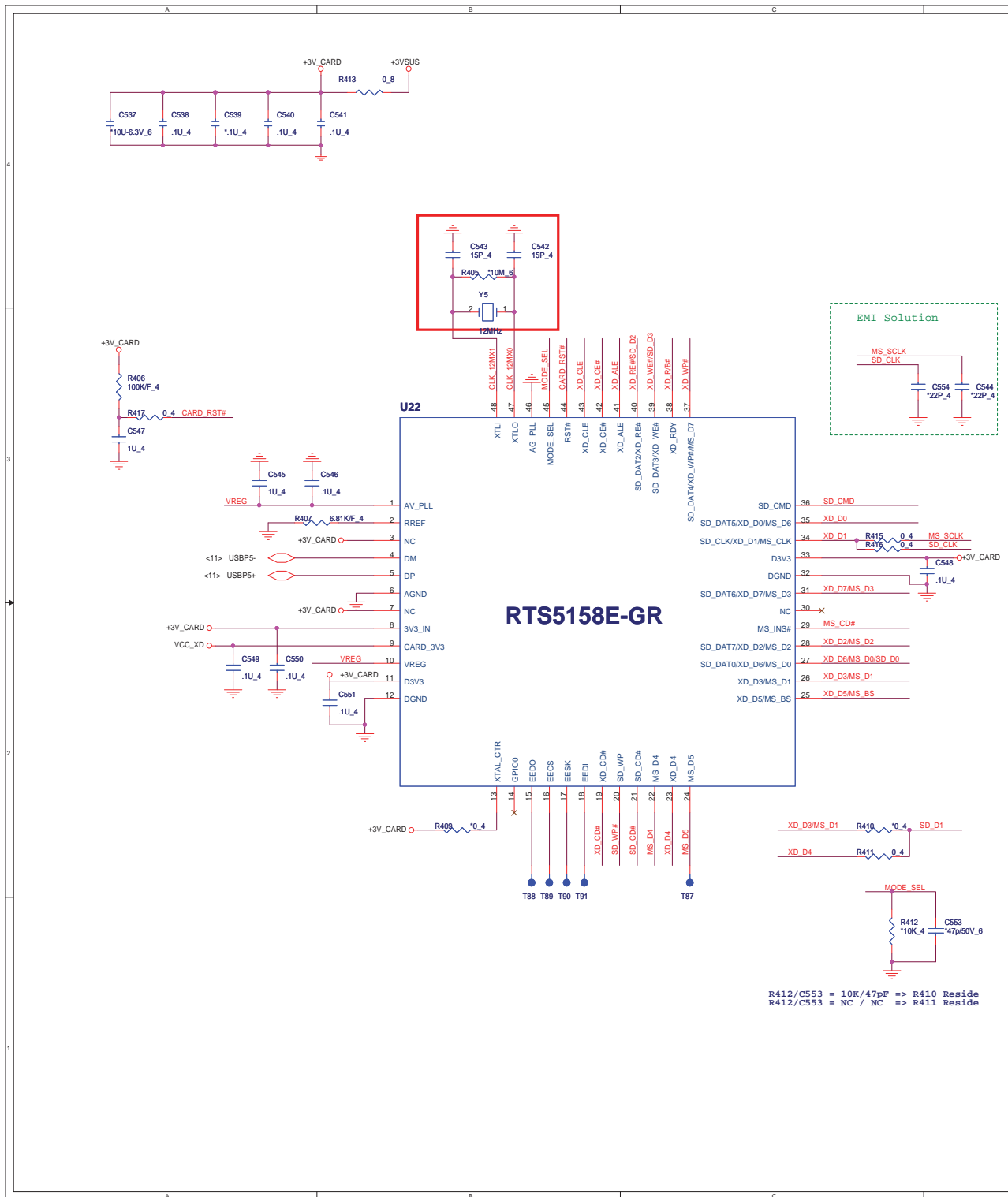
## ODD (SATA)



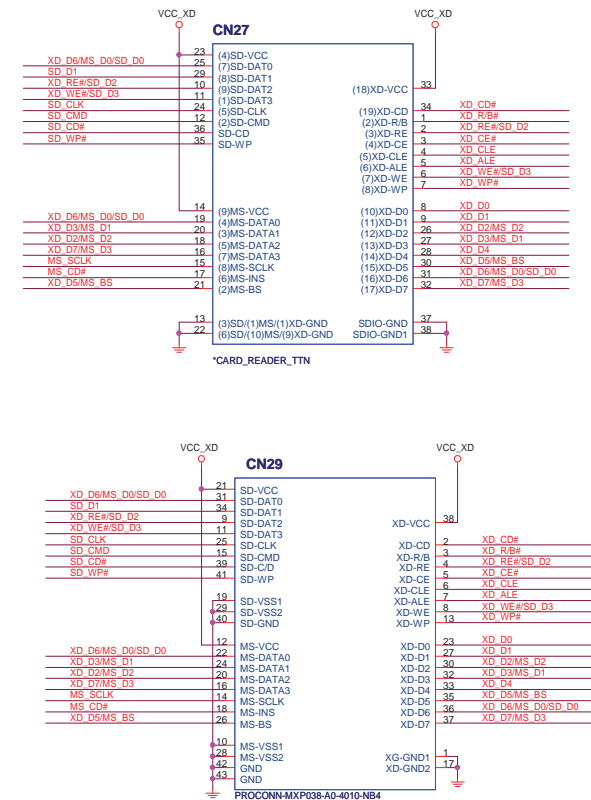
Quanta Computer Inc.

PROJECT : Z05

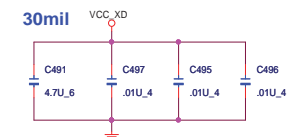
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	SATA-HDD & SATA-ODD&TP	1A
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## 7 IN 1 CARD READER



## CARDREADER POWER



The circuit diagram shows a precision current source using the AD5040. The circuit is powered by a +5V supply. A 1.2V reference voltage is applied to the REF pin. The output current is set by a feedback resistor R371. The output voltage is measured across a load resistor R171. The circuit includes several capacitors (C306, C309, C318, C312, C313, C316) and a resistor network (R191, R371, R372) to stabilize the output.

The output voltage is calculated as:

$$V_o = 1.2 \cdot (R371 + R372) / R371 = 4.8V$$

AGC_Attack (4 pin)	Attack time
LOW	1 ms
Hi	2 ms

### AGC ON/OFF selection

AGC_ON/OFF (6 pin)	AGC ON/OFF
LOW	ON
Hi	OFF

AGC_Recovery1 (10 pin)	AGC_Recovery2 (11 pin)	Recovery Time
LOW	LOW	1.0 s
LOW	HI	2.0 s
HI	LOW	4.0 s
HI	HI	8.0 s

AGC_Lv1 (2 pin)	AGC_Lv2 (3 pin)	AGC ON Level	Output Po (RL=8 ohm)
LOW	LOW	9.8 dBV	1.2 W
LOW	Hi	9.0 dBV	1.0 W
Hi	LOW	8.1 dBV	0.8 W
Hi	Hi	6.0 dBV	0.5 W

SP_STBY1 (33 pin)	SP_STBY2 (34 pin)	SP_STBY ON/OFF
LOW	LOW	ON
LOW	HI	OFF
HI	LOW	OFF
HI	HI	OFF

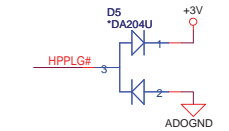
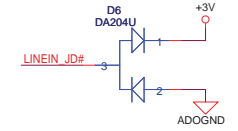
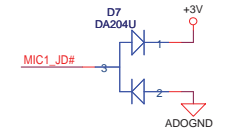
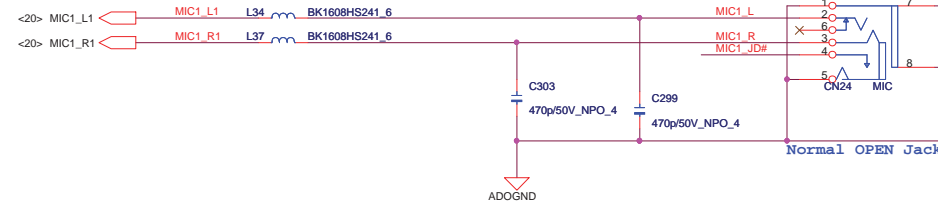
HP_STBY1 (35 pin)	HP_STBY2 (36 pin)	HP_STBY ON/OFF
LOW	LOW	ON
LOW	HI	OFF
HI	LOW	OFF
HI	HI	OFF

The diagram illustrates the internal circuitry of the AN12948A component, which is a Panasonic U17 IC. The IC is shown with its pins connected to various power and signal sources. Key connections include:

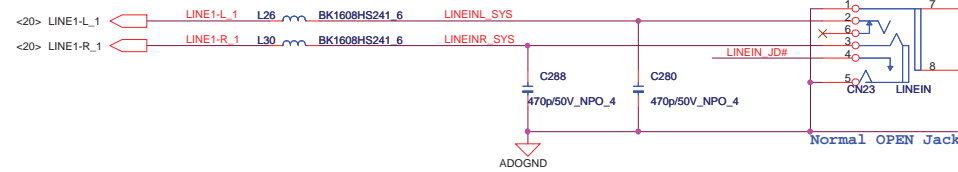
- Power Supply:** The IC is powered by a +3V AVDD and +5V VDD. The VCC\_CP pin is connected to the +3V AVDD, and the VCC\_HP pin is connected to the +5V VDD. The VSS\_CP pin is connected to the VSS.
- Signal Pins:** The IC has several signal pins, including AGC\_Lv1, AGC\_Lv2, AGC\_Attack, AGC\_ON/OFF, AGC\_Recovery1, AGC\_Recovery2, SP\_INL, SP\_OUTL, SP\_OUTR, SP\_OUT+, SP\_OUT-, HP\_OUTL, HP\_INL, HP\_INR, and HP\_OUTR. These pins are connected to various external components, including capacitors (C492, C494, C498, C499) and resistors (R360, R361, R359, R358).
- Grounding:** The IC is grounded to ADOGND and CPGND. The CPGND pins (CPGND\_1, CPGND\_2, CPGND\_3) are connected to the CPGND\_1, CPGND\_2, and CPGND\_3 pins of the HP module.
- HP Module:** The HP module is connected to the HP\_OUTL, HP\_INL, HP\_INR, and HP\_OUTR pins of the IC. The HP module also has its own power and ground pins (VCC, VSS, GND, HP, SURR-R).

The diagram is a detailed schematic of the AN12948A circuit, showing the internal components and their connections to the HP module. The IC is a Panasonic U17, and the circuit is designed to provide a high-performance audio output to the HP module.

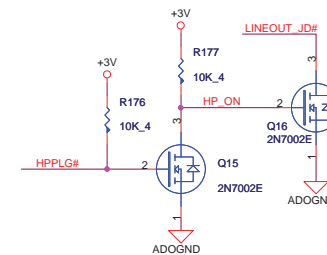
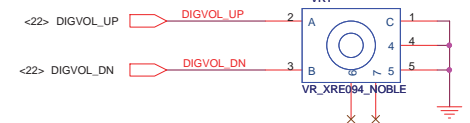
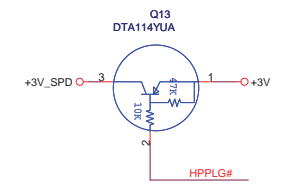
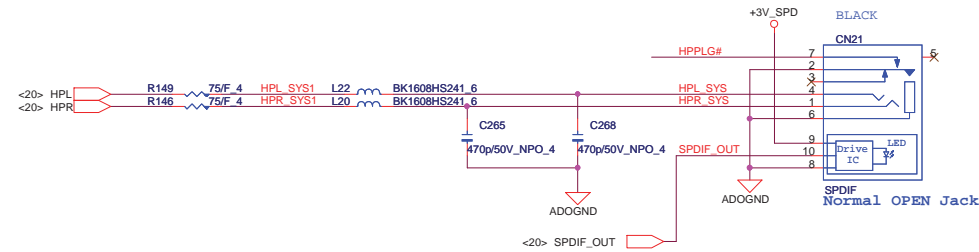
## MIC



## LINE IN



## HeadPhone OUT/SPDIF



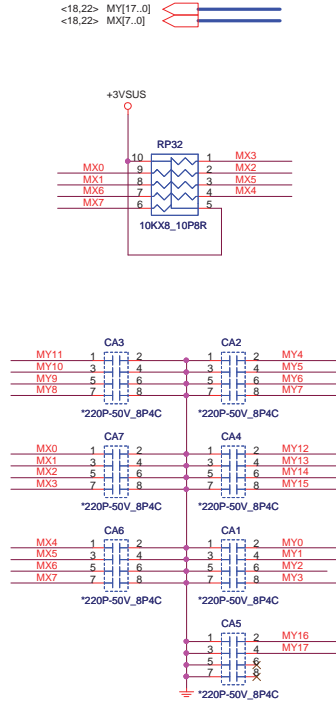




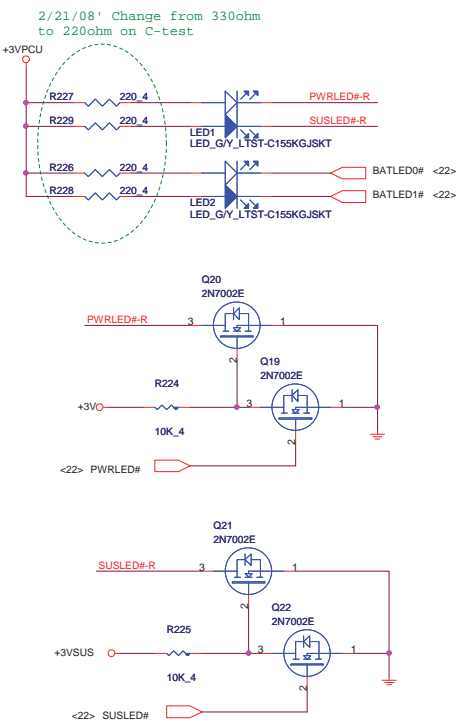
## INT K/B

CN4	
1	MY0
2	MY1
3	MY2
4	MY3
5	MY4
6	MY5
7	MY6
8	MY7
9	MY8
10	MY9
11	MY10
12	MY11
13	MY12
14	MY13
15	MY14
16	MY15
17	MY16
18	MY17
19	MX7
20	MX6
21	MX5
22	MX4
23	MX3
24	MX2
25	MX1
26	MX0

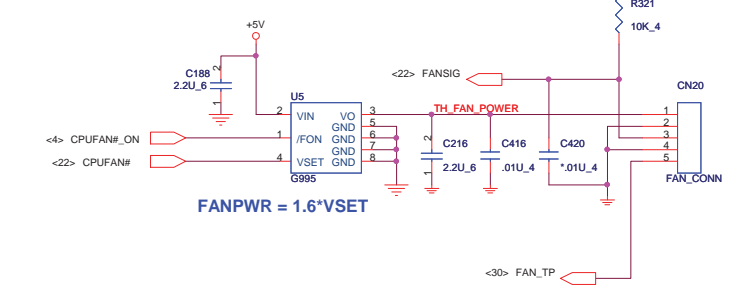
FFC\_26P\_KB



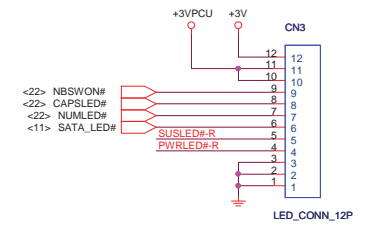
## LED



## CPU FAN



## LED BOARD CONN.



## Debug

Delete Debug Port(PCI & IDE)

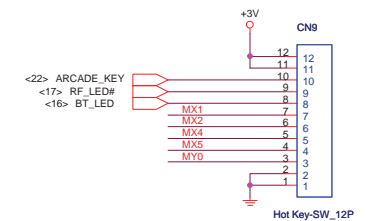
## Fingerprint BOARD CONN.

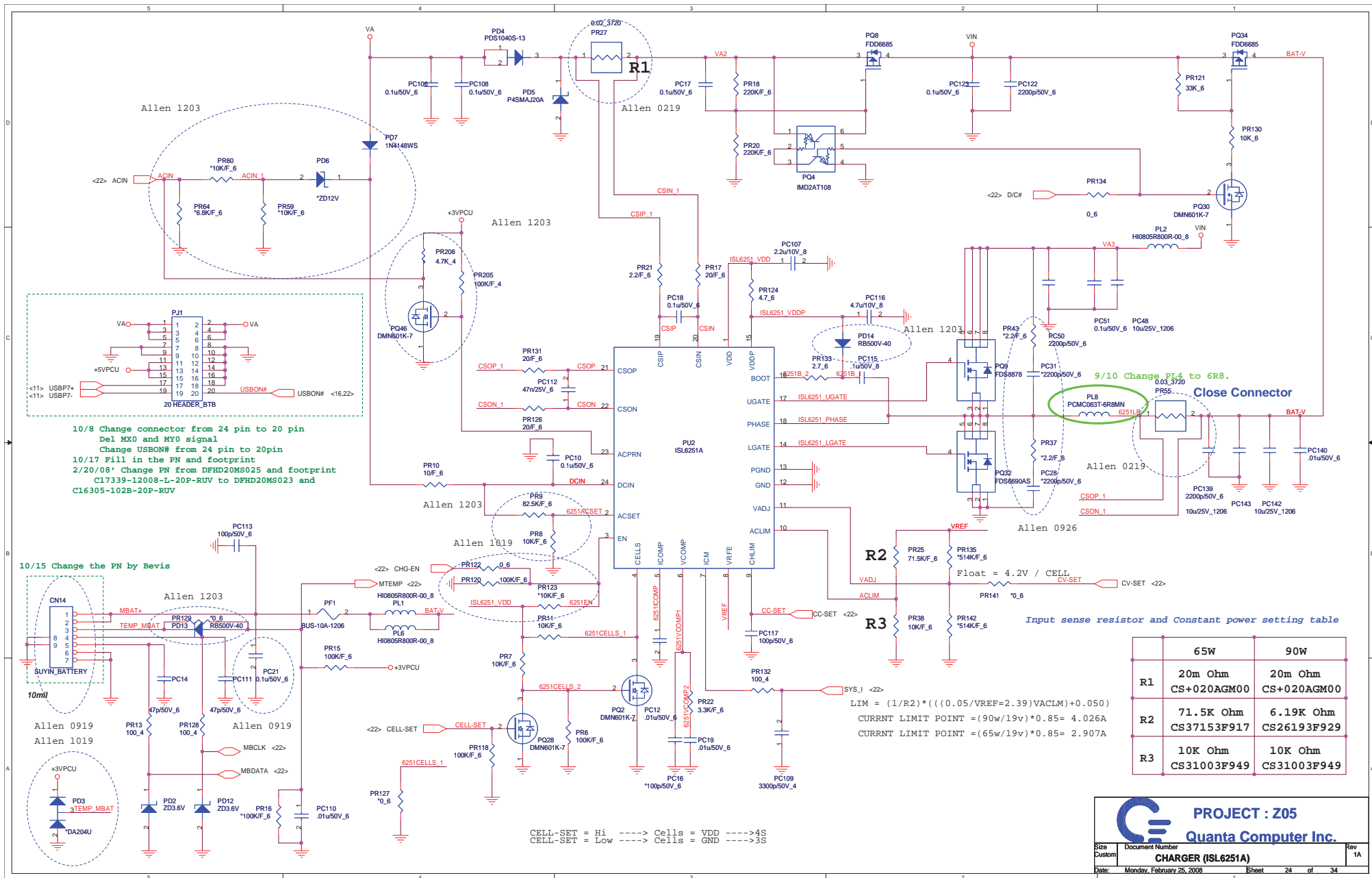


## Button BOARD CONN.

### BUTTON MATRIX

	MY0
MX1	MAIL
MX2	WWW
MX4	WIRELESS
MX5	BLUETOOTH







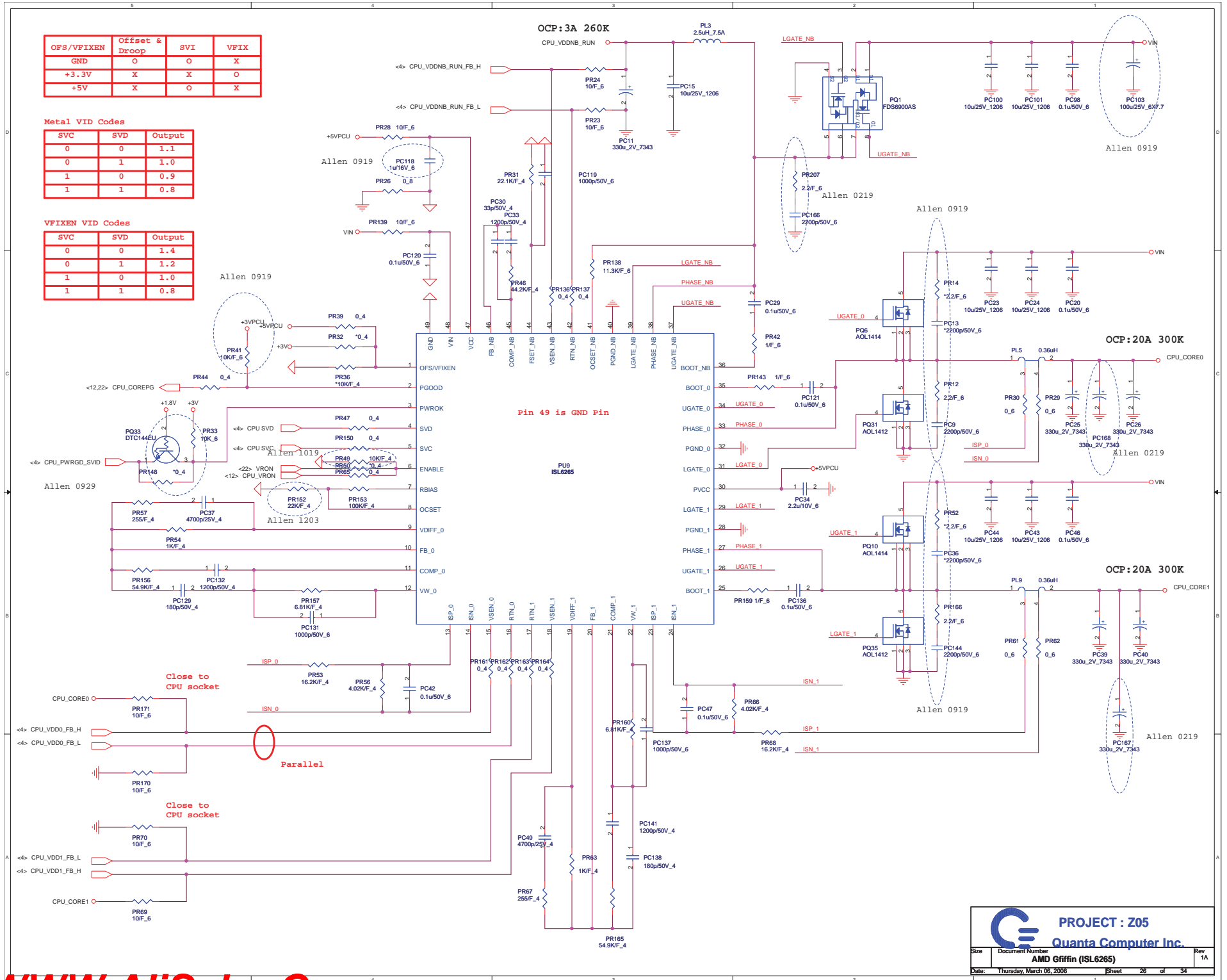
OFS/VFIXEN	Offset & Droop	SVI	VFIX
GND	O	O	X
+3.3V	X	X	O
+5V	X	O	X

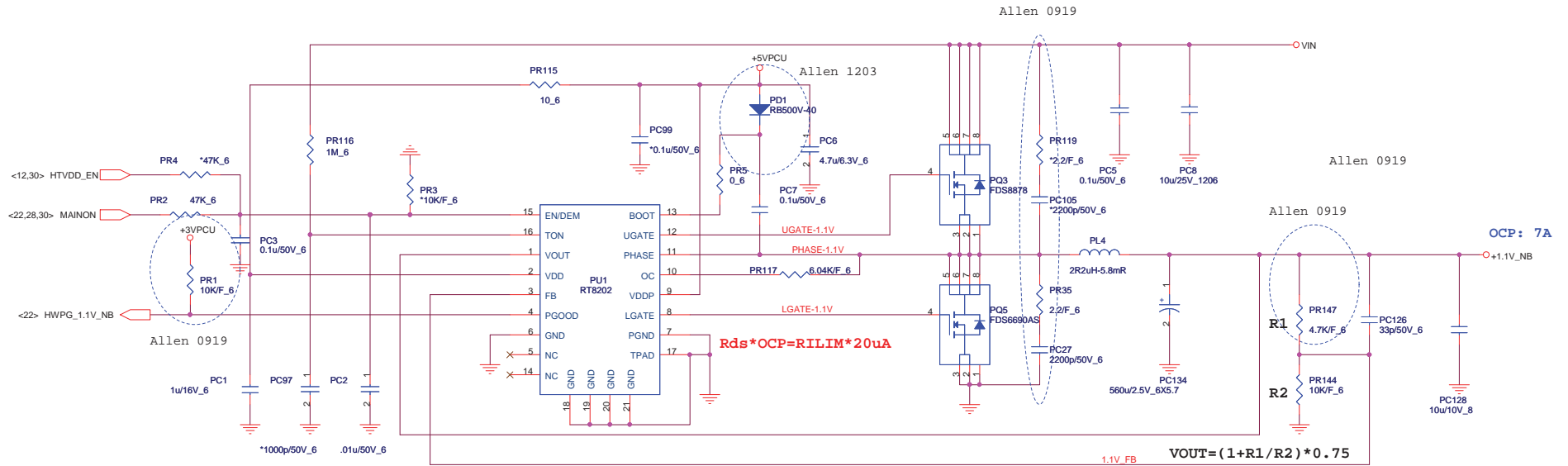
Metal VID Codes

SVC	SVD	Output
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

VFIXEN VID Codes

SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8





$$TON = 3.85p * RTON * Vout / (Vin - 0.5)$$

$$Frequency = Vout / (Vin * TON)$$

$$TON = 3.85p * 1M * 1 / (Vin - 0.5)$$

$$Frequency = 1 / (0.0036767) = 272K$$

$$FDS6690AS \ R_{ds} = 12-15m\Omega$$

$$OCP = 7-0.8A$$

$$L(\text{ripple current}) = (19-1) * 1 / (2.2u * 272k * 19) \sim 1.58A$$

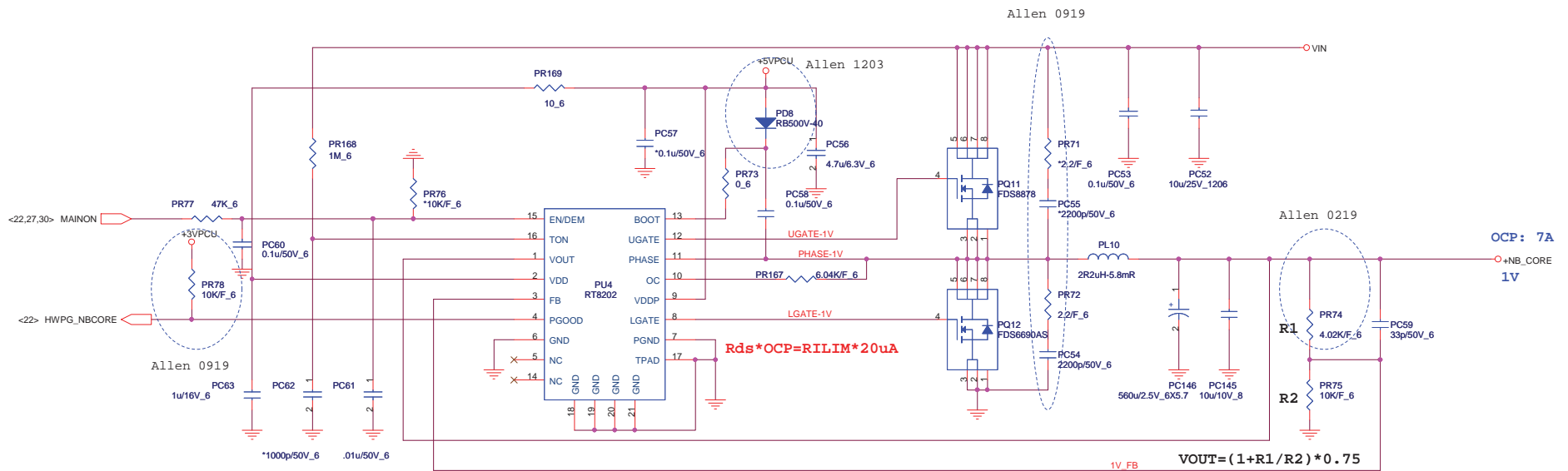
$$12m * 6 = RILIM * 20\mu A$$

$$RILIM = 3.6K (2.5-8K)$$



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$$TON = 3.85p * RTON * Vout / (Vin - 0.5)$$

$$Frequency = Vout / (Vin * TON)$$

$$TON = 3.85p * 1M * 1 / (Vin - 0.5)$$

$$Frequency = 1 / (0.0036767) = 272K$$

FDS6690AS Rds=12~15mOhm

OCP=7~0.8A

L(ripple current)  
 $= (19-1) * 1 / (2.2u * 272k * 19)$   
 ~1.58A

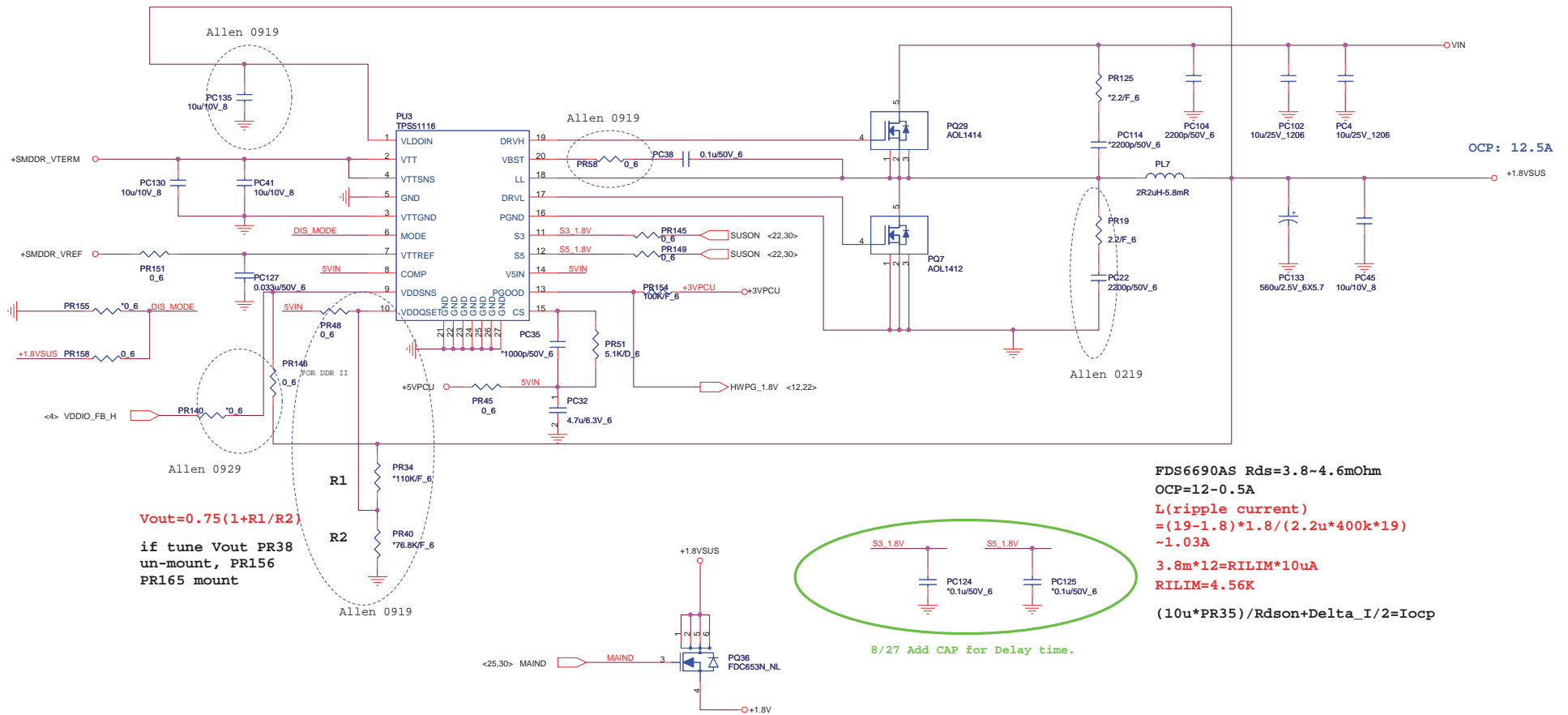
12m\*6=RILIM\*20uA

RILIM=3.6K(2.5~8K)



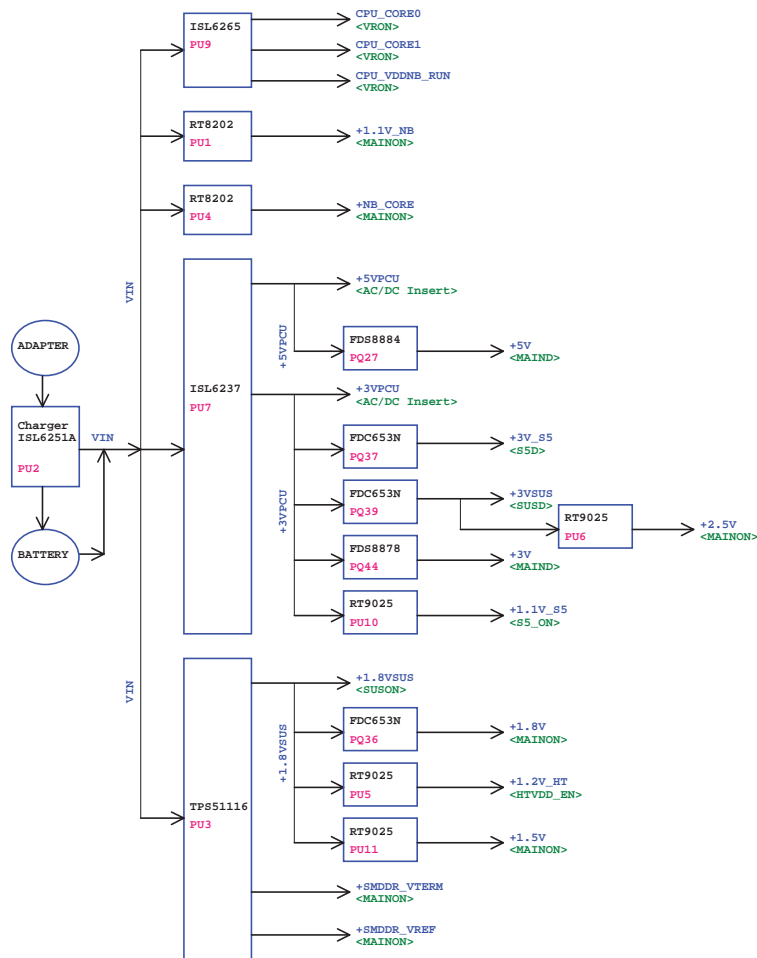
PROJECT : Z05  
 Quanta Computer Inc.

Size	Document Number	Rev
	NB_VCC (RT8202)	1A
Date:	Monday, February 25, 2008	Sheet 28 of 34









1. +1.1V\_S5MCP77M Power(+1.1V\_DUAL)
2. +5VPCUPower IC VCC, USB PORT POWER(S3 control)
3. +5VAudio, FAN, Touch pad, SATA HDD, ODD, CRT
4. +3V\_S5MCP77M, New Card, LAN Power
5. +3VPCUKBC WPCE755C,SPI ROM, LED, LID Switch, Fingerprint Module
6. +3VSUSBluetooth, Mini Card, MDC
7. +3VCPU Thermal Sense, MCP77M, System Memory, LCD Panel, PC Camera, Mini card, New Card, Audio, Codec, Card Reader, KBC WPCE775C, LED
8. +2.5VPCPU VDDA
9. +3V\_LANLAN Power(BCM5764M)
10. +1.2V\_LANLAN Power(BCM5764M)
11. +2.5V\_LANLAN Power(BCM5787M)
12. +1.5VMini Card, New Card
13. +1.8VSUSCPU VDD I/O, System Memory
14. SMDDR\_VTEMCPU Memory Interface , SYSTEM DDR DIMM Memory Termination
15. +1.8VMCP77M LCD Interface
16. +1.1V\_NBMCP77M (HT Interface, PCI-E Interface, I/O Power, SATA Interface)
17. +NB\_COREMCP77M Core Power
18. +1.2V\_HTCPU HT Power
19. CPU\_CORE0 CPU Power
20. CPU\_CORE1 CPU Power
21. CPU\_VDDNB\_RUNCPU NB Power
- 22.